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Patentanmeldung Nr. Patent application No. Demande de brevet n°

04101071.1

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(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
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Method of manufacturing a semiconductor device and semiconductor device obtained with such a method

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Method of manufacturing a semiconductor device and semiconductor device obtained with such a method

The invention relates to a method of manufacturing a semiconductor device comprising a field effect transistor, in which method a semiconductor body of silicon is provided at a surface thereof with a source region and a drain region of a first conductivity type which both are provided with extensions and with a channel region of a second conductivity type, opposite to the first conductivity type, between the source region and the drain region and with a gate region separated from the surface of the semiconductor body by a gate dielectric and situated above the channel region and wherein a pn-junction between the extensions and a neighboring part of the channel region is formed by two implantations of dopants of opposite conductivity type and wherein before both of said two implantations of opposite conductivity type dopants are performed an amorphizing implantation is done where the pn-junction is to be formed. Such a method is very suitable for making MOSFET (= Metal Oxide Semiconductor Field Effect Transistor) devices. The amorphizing implantation helps to prevent channeling of subsequently implanted dopants and thus contributes to obtaining a steeper pn-junction.

A method as mentioned in the opening paragraph is known from US patent US 6,268,640 B1 that has been issued on July 31, 2001. Therein (see figure 6 and columns 3 to 5) a method is described in which shallow extensions of source and drain are formed by implanting suitable dopants into the semiconductor body and in which in addition a so-called pocket dopant layer, of an opposite conductivity type, is formed around the extensions by an implantation of opposite conductivity type dopants. Before both above-mentioned implantations, an amorphizing implantation of e.g. Ge or Si is done in the region around the pn-junction formed between the source- and drain extensions and a neighboring part of channel region, in this case the pocket region. As mentioned before, such an implant helps in avoiding channeling of the subsequently opposite conductivity type implantations and thus contributes to obtaining a steeper pn-junction. In order to form the pn-junction below the gate, the above US patent teaches to do the amorphizing implantation as well as the two opposite conductivity implantations with a tilt, i.e. at an non-zero angle with the normal of

the surface of the semiconductor body. The above mentioned implantations are subsequently annealed at a temperature in the range of 900 to 1050 degrees Celsius.

A drawback of such a method is that on the one hand the shallowness and steepness of the pn-junction to be formed as well as the electrical quality thereof are still not sufficient for future CMOS devices, in particular diode leakage current of the pn-junction is too high.

It is therefore an object of the present invention to avoid the above drawbacks and to provide a method which does provide satisfactory results for very small devices and by which a very shallow and steep pn-junction is obtained with an excellent electrical quality and thus with a low (diode) leakage current.

To achieve this, a method of the type described in the opening paragraph is characterized in that the amorphizing implantation and said two implantations of dopants of opposite conductivity type are done before the gate region is formed and at an angle with the surface of the semiconductor body which is substantially equal to 90 degrees. The present invention is firstly based on the recognition that the increased diode leakage is the result of defects in the material of the semiconductor body which are introduced by the amorphizing implantation and which are present at the end of the projected range of said implantation. If such an implantation is done with a tilt, such defects are present also in the neighborhood of the vertical part (i.e. the part perpendicular to the surface of the semiconductor body) of the pn-junction to be formed. The latter part is most critical with respect to its contribution to the leakage current associated with the diode formed by the pn-junction. Furthermore, the invention is based on the recognition that if said implantation is done before the gate is formed, it may easily be done in a direction perpendicular to the surface of the semiconductor body. Furthermore, by doing also the two opposite conductivity type implantations before the gate is formed and at an angle substantially perpendicular to the surface of the semiconductor boy, the steepness of said vertical part of the pn-junction to be formed is improved. Thus, in a device obtained with a method according to the present invention, said vertical part of the pn-junction is of very high electrical quality and moreover very steep. It is to be noted that the neighboring part of the channel region does not necessarily has to be a so-called pocket region. The only requirement is that said region forms a pn-junction with the channel region and the opposite conductivity type source and drain regions.

In a first embodiment of a method according to the invention a first implantation of said two opposite conductivity type implantations is done using a first mask covering a first region of the semiconductor body and the second implantation is done after removal of the first mask using a second mask of which the edge coincides with the edge of the first mask. Although one of the two implantations might be done in a larger area and the other one with a mask of which the edge is positioned above said area, this embodiment in which the two implantations border each other provides more freedom in choosing the doping concentrations as no overcompensating is needed. In particular the doping concentrations may be about equally large. This also contributes to the steepness of said vertical part of the pn-junction. Preferably, the first mask and second mask are formed in a self-aligned manner. In this way the vertical part of the pn-junction is very steep and it is avoided that a region is present at the location of the pn-junction which is not doped by either of the two opposite conductivity type implantations.

In a preferred embodiment of a method according to the invention the first mask is formed by a dummy gate region of a first dielectric material and the first implantation is used to form the extensions of the source and drain regions. Such a method allows for a good positioning of the source and drain extensions with respect to the gate provided the gate region is formed at the same location as the dummy gate region. The latter is possible as will be shown by a further embodiment.

Preferably after the first implantation a uniform masking layer of a second dielectric material different from the first dielectric material is deposited on the semiconductor body which subsequently is removed by chemical mechanical polishing on top of the dummy gate region which then is removed by selective etching, the remainder of the masking layer forming the second mask for the second implantation which is used to dope the neighboring part of the channel region. In this way, the implantation of the two opposite conductivity type implantation used to form the (vertical part of the) pn-junction, by implanting a neighboring part of the channel region, is formed in a self-aligned manner with respect to the source- and drain extensions.

A favorable modification is characterized in that after the second implantation a uniform gate region layer is formed on top of the semiconductor body which subsequently is removed by chemical mechanical polishing on top of the second mask which is then removed by selective etching. In this way the gate region becomes self-aligned with both the position of the source- and drain extensions an the neighboring part of the implantation. Of course the gate region should contain at its bottom a dielectric region. The latter may be

included in the gate region layer if the dielectric region is formed by deposition. Another possibility in which the dielectric region is formed e.g. by oxidation of the silicon surface, such an oxidation may be done before the gate region layer is deposited. It may be formed, self-aligned just before of after the second implantation using the window formed by removal of the dummy gate. In these cases, the gate region layer does not necessarily include a dielectric part but may merely comprise e.g. a polysilicon layer of a metal layer if a metal gate is desired.

In another preferred embodiment of a method according to the invention the first and second implantations (I_1, I_2) are annealed at a temperature between 500 en 700 degrees Celsius. In this way, both the horizontal and vertical part of the pn-junction are formed by solid phase epitaxial re-growth. This greatly contributes to the shallowness and steepness of the pn-junction formed, which in turn is essential for future C-MOS technology.

Preferably, the (deeper) source- and drain regions themselves are formed before the formation of the source- and drain extensions and the pn-junction thereof with the part of the channel region neighboring the source- and drain extensions. In this way, the source- and drain regions may be formed at a higher temperature, e.g. by implantation followed by an anneal at a temperature well above 700 degrees Celsius.

For the amorphizing implantation not only ions like Ge or Si ions may be used but also ions of an inert gas like Ar or Xe can be used advantageously. Also dopants that "self-amorphize" may be considered, e.g. As, P and Sb. The self-amorphizing effect of an implantation of these impurities occurs above a certain implantation energy and also depends on the implantation flux. In particular in case of As ions are, it has been found that it is advantageous to take over a part of the amorphizing implantation by the As implantation itself. In a modification of the above embodiments in accordance with this principle, the amorphizing implantation by means of Ge, Si or Ar, Xe is done after placing the first mask and than the first doping implantation (I_1) is done which in this case is a p-type implantation. Afterwards the first mask is removed and the second mask is placed. Then the second doping (I_2) in this case an As implantation is performed which is self-amorphizing.

The invention further comprises a semiconductor device with a field effect transistor which is obtained with a method according to the invention. In such a device the pocket region may have a very abrupt and narrow doping profile.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter, to be read in conjunction with the drawing, in which

Figs. 1 through 9 are sectional views of a semiconductor device with a field effect transistor at various stages in the manufacture of the device by means of a method in accordance with the invention.

The figures are diagrammatic and not drawn to scale, the dimensions in the thickness direction being particularly exaggerated for greater clarity. Corresponding parts are generally given the same reference numerals and the same hatching in the various figures.

Figures 1 through 9 are sectional views of a semiconductor device with a field effect transistor at various stages in the manufacture of the device by means of a method in accordance with the invention. The method for forming a device 10 starts (see figure 1) in this example with a substrate 11 which in this case, but not necessarily, comprises silicon and thus also forms part of the semiconductor body 1 of silicon and which in this example is of the p-type conductivity. It is to be noted here that the substrate 11 also can have the opposite conductivity type. Moreover, the region 11 may also be e.g. an n-well (or p-well for that matter) within a silicon substrate of the opposite conductivity type, e.g. p-type and n-type respectively. Furthermore, the substrate / region 11 comprises the channel region 4 of the transistor to be formed. The device 10 to be formed, which is in this case a NMOST, contains in practice near its borders isolation regions 12 such as a so-called trench or LOCOS (= Local Oxidation of Silicon) isolation, which are formed in a conventional manner. In practice the device 10 will contain many transistors in a CMOS device 10 both of the NMOS and PMOS type.

At the surface of the semiconductor body 1 a mask 13 is formed by photolithography if desired after deposition of a dielectric material which then comprises a photoresist or a dielectric respectively. The mask 13 is used to form the source- and drain regions 2,3 of the transistor to be formed, in this case by means of a ion implantation $I_{S,D}$ of n-type dopants like As ions followed by a high temperature anneal at a temperature above 900 degrees Celsius.

After removal of the mask 13 (see figure 2) an amorphizing implantation I_0 is performed in this example of Si ions. The resulting amorph silicon region near the surface of the semiconductor body 1 is not indicated separately in the drawing.

Next (see figure 3) a dummy gate region 5A is formed by deposition of a layer of a first dielectric material like silicondioxide which is patterned by means of photolithography and etching into a first mask M1 which comprises the dummy gate region 5A. The mask M1 is used for a first ion implantation I_1 of in this case n-type impurities like As ions. In this way, shallow source- and drain extensions 2A,3A are formed.

Subsequently (see figure 4) a layer 40 comprising a second, different, dielectric material, in this case siliconnitride is deposited uniformly over the surface of the semiconductor body 1. Hereinafter (see figure 5) said layer 40 is partly removed by chemical-mechanical polishing such that the mask M1 is freed of said layer 40. The remaining part of the masking layer 40 forms a second mask M2. Next (see figure 6) the first mask M1 is removed by etching selective with respect to the second mask M2. Then, a second ion implantation I_2 is done with ions of impurities that form the second (opposite) conductivity type e.g. with B ions. In this way a region 4A of the channel region 4 is formed which borders the source- and drain extensions 2A,3A.

Thanks to the method according to invention the vertical part of the pn-junction formed – after an annealing step to be discussed hereinafter - between the region 4A of the channel region 4 and the source- and drain extensions 2A,3A is one the one hand very steep and abrupt and on the other hand has excellent diode properties like a low leakage current, the latter being due to the fact that there are no or at least very little defects present in the semiconductor body 1 in the surface regions that border said vertical part of said pn-junction.

Next (see figure 7) a gate region forming layer 50,60 is deposited on top of the semiconductor body in this example by means of CVD (= Chemical Vapor) deposition. In this example the said gate region forming layer 50,60 comprises a thin dielectric region layer 60 and a thicker polysilicon layer 60.

Hereinafter (see figure 8) the semiconductor body 1 is again treated by chemical-mechanical polishing in order to locally remove said gate region layer 50,60 above the second mask M2. The remaining parts of said layer 50,60 form the gate dielectric 6 and the in this case polysilicon gate 5 of the transistor to be formed.

Next (see figure 9) the second mask M2 is removed by (selective) etching. The surface of the semiconductor body 1 outside the gate region 5,6 will be covered and protected by a dielectric layer, e.g. of silicondioxide, which is not indicated in the drawing and which may be present at a stage in the manufacturing in which this mask may be applied.

Next the amorphous silicon resulting from the opposite conductivity type implantations (I_1, I_2) but essentially from the amorphizing implantation (I_0) is recovered in an annealing process between a temperature between 500 and 700 degrees Celsius, preferably between 550 and 650 degrees Celsius. I

Finally the manufacturing of the n-MOSFET is further completed by deposition of a pre-metal dielectric, e.g. of silicondioxide, followed by patterning thereof , deposition of a contact metal layer, e.g. of aluminum, again followed by patterning by which contact regions are formed. These steps are not shown in the drawing. A (self-aligned) silicide process may further be used to contact the source- and drain regions 2,3 and the gate region 5.

It will be obvious that the invention is not limited to the examples described herein, and that within the scope of the invention many variations and modifications are possible to those skilled in the art.

CLAIMS:

1. Method of manufacturing a semiconductor device (10) comprising a field effect transistor, in which method a semiconductor body (1) of silicon is provided at a surface thereof with a source region (2) and a drain region (3) of a first conductivity type which both are provided with extensions (2A,3A) and with a channel region (4) of a second conductivity type, opposite to the first conductivity type, between the source region (2) and the drain region (3) and with a gate region (5) separated from the surface of the semiconductor body (1) by a gate dielectric (6) and situated above the channel region (4) and wherein a pn-junction between the extensions (2A,3A) and a neighboring part (4A) of the channel region (4) is formed by two implantations (I_1 , I_2) of dopants of opposite conductivity type and wherein before both of said two implantations (I_1 , I_2) of opposite conductivity type dopants are performed an amorphizing implantation (I_0) is done where the pn-junction is to be formed, characterized in that the amorphizing implantation (I_0) and said two implantations (I_1 , I_2) of dopants of opposite conductivity type are done before the gate region (5) is formed and at an angle with the surface of the semiconductor body (1) which is substantially equal to 90 degrees.

2. Method according to claim 1, characterized in that a first implantation (I_1) of said two opposite conductivity type implantations (I_1 , I_2) is done using a first mask (M1) covering a first region of the semiconductor body (1) and the second implantation (I_2) is done after removal of the first mask (M1) and using a second mask (M2) of which the edge coincides with the edge of the first mask (M1).

3. Method according to claim 2, characterized in that the first mask (M1) and the second mask (M2) are formed in a self-aligned manner.

4. Method according to claim 2 or 3, characterized in that the first mask (M1) is formed by a dummy gate region (5A) of a first dielectric material and the first implantation (I_1) is used to form the extensions (2A,3A) of the source and drain regions (2,3).

5. Method according to claim 4, characterized in that after the first implantation (I_1) a uniform masking layer (40) of a second dielectric material different from the first dielectric material is deposited on the semiconductor body (1) which subsequently is removed by chemical mechanical polishing on top of the dummy gate region (5A) which then is removed by selective etching, the remainder of the masking layer (40) forming the second mask (M2) for the second implantation (I_2) which is used to dope the neighboring part (4A) of the channel region (4).

6. Method according to claim 5, characterized in that after the second implantation (I_2) a uniform gate region layer (50) is formed on top of the semiconductor body (1) which subsequently is removed by chemical mechanical polishing on top of the second mask (M2) which is then removed by selective etching.

7. Method as claimed in anyone of the preceding claims, characterized in that the first and second implantations (I_1 , I_2) are annealed at a temperature between 500 en 700 degrees Celsius

8. Method as claimed in anyone of the preceding claims, characterized in that the source- and drain regions (2,3) are formed before the source- and drain extensions (2A,3A).

9. Method as claimed in anyone of the preceding claims, characterized in that for the amorphizing implantation (I_0) ions are chosen from a group comprising Ge, Si, Ar or Xe.

10. Method as claimed in anyone of the preceding claims, characterized in that a part of the function of the amorphizing implantation (I_0) is provided by one of the two opposite conductivity type implantations (I_1 , I_2).

11. A semiconductor device (10) comprising a field effect transistor obtained with a method as claimed in anyone of the preceding claims.

ABSTRACT:

The invention relates to a method of manufacturing a semiconductor device (10) comprising a field effect transistor, in which method a semiconductor body (1) of silicon is provided at a surface thereof with a source region (2) and a drain region (3) of a first conductivity type which both are provided with extensions (2A,3A) and with a channel region (4) of a second conductivity type, opposite to the first conductivity type, between the source region (2) and the drain region (3) and with a gate region (5) separated from the surface of the semiconductor body (1) by a gate dielectric (6) and situated above the channel region (4) and wherein a pn-junction between the extensions (2A,3A) and a neighboring part (4A) of the channel region (4) is formed by two implantations (I_1 , I_2) of dopants of opposite conductivity type and wherein before said two implantations (I_1 , I_2) of opposite conductivity type dopants an amorphizing implantation (I_0) is done where the pn-junction is to be formed.

According to the invention the method is characterized in that the amorphizing implantation (I_0) and said two implantations (I_1 , I_2) of dopants of opposite conductivity type both are done before the gate region (5) is formed and at an angle with the surface of the semiconductor body (1) which is substantially equal to 90 degrees. In this way, the most relevant part of the pn-junction that is formed, i.e. the vertical part that runs perpendicular to the surface, is not only very steep and abrupt but also has a very low leakage current due to the absence of implantation defects. In a preferred embodiment said two opposite conductivity type implantations (I_1 , I_2) are localized in a self-aligned manner. Preferably, a low temperature anneal is to used to re-grow crystalline silicon.

Fig. 6

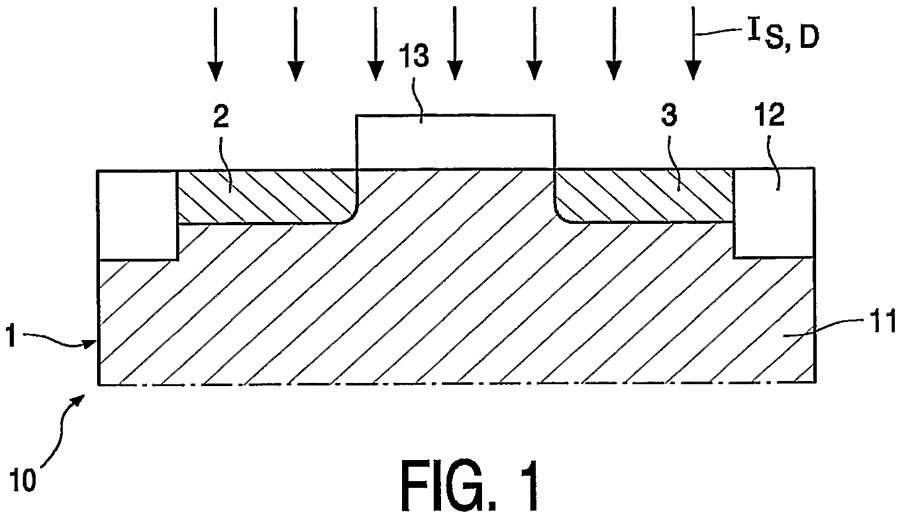


FIG. 1

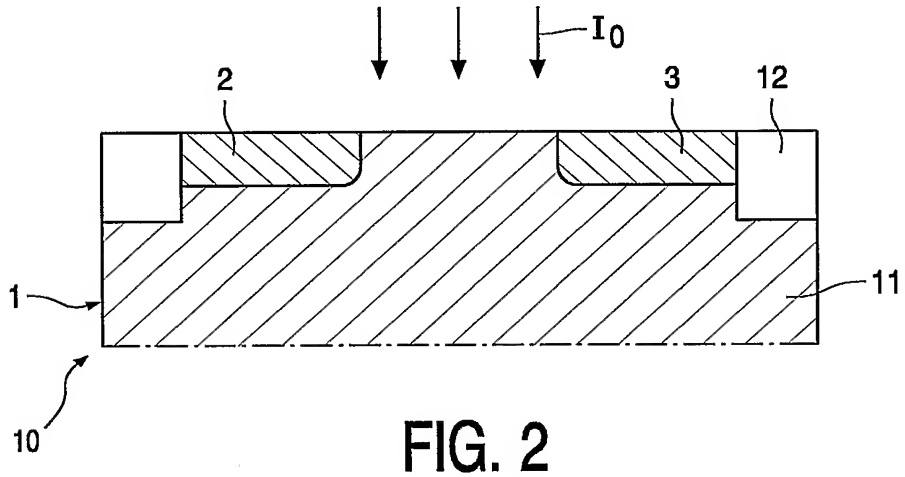


FIG. 2

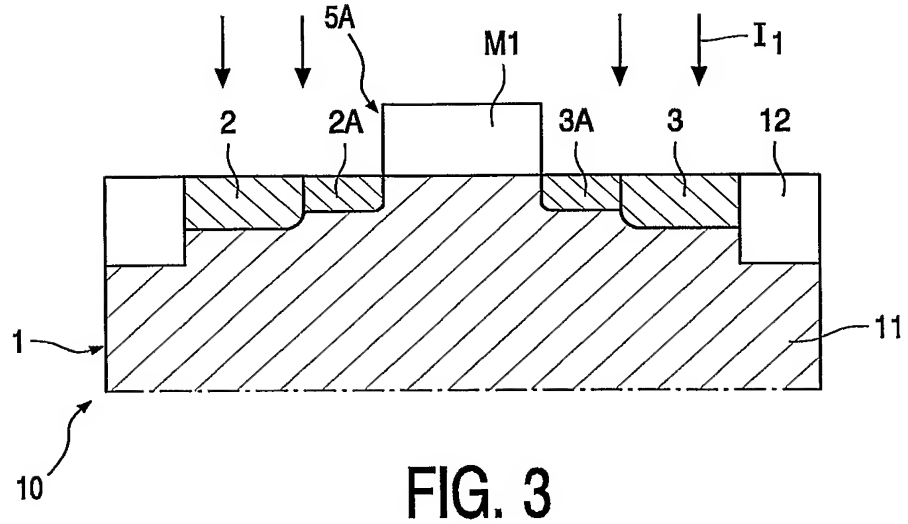


FIG. 3

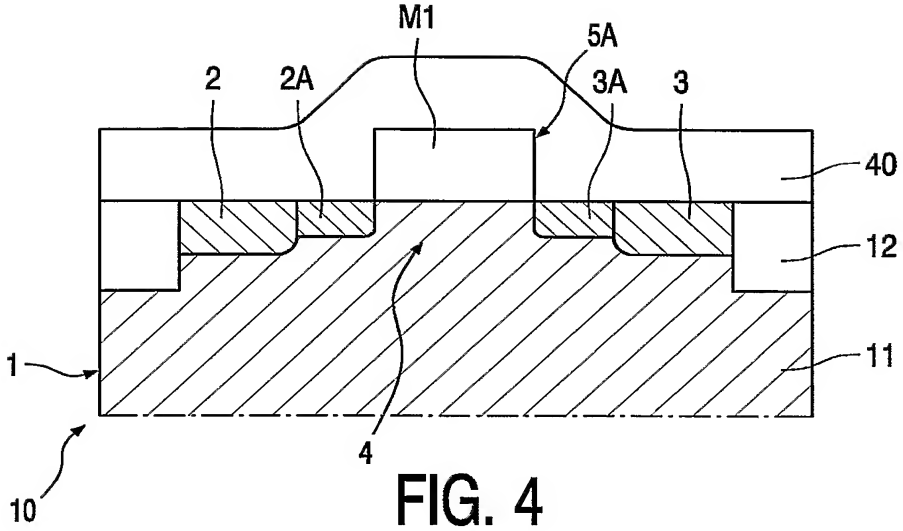

M1
5A
2
2A
3A
3
40
12
1
11
4
10

FIG. 4

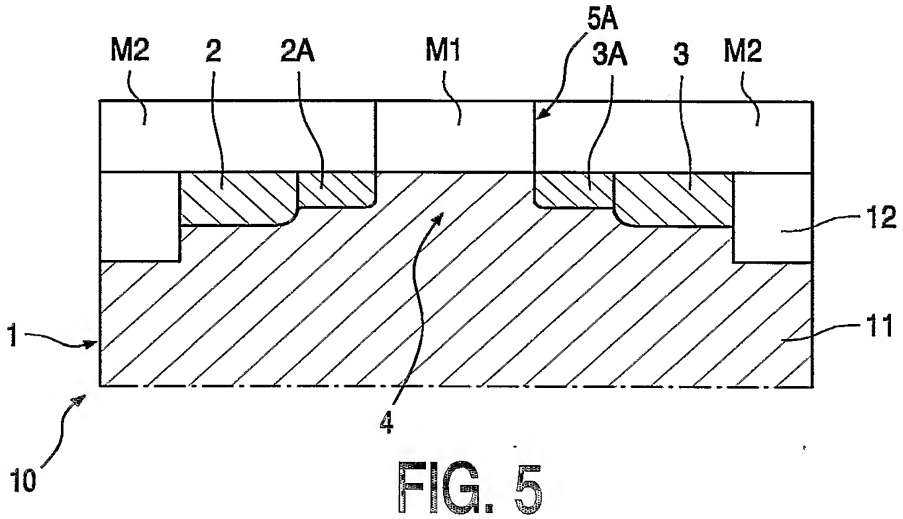
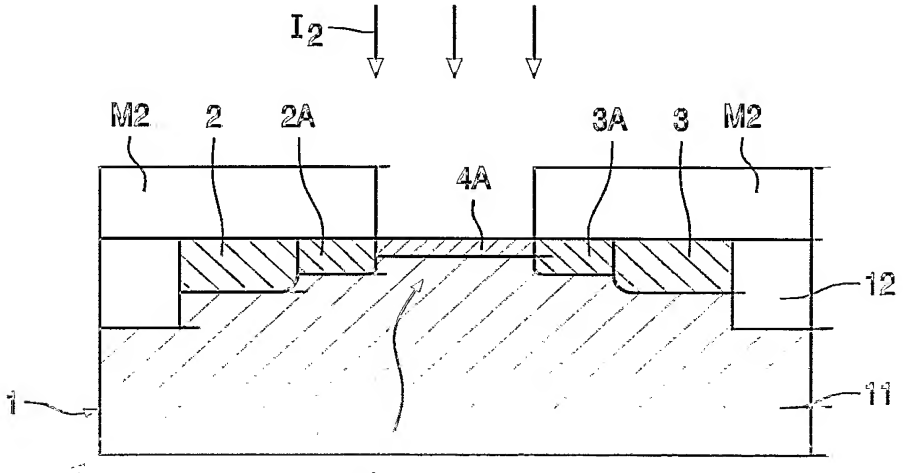

5A
M2
2
2A
M1
3A
3
M2
12
1
11
4
10

FIG. 5


I2
M2
2
2A
3A
3
M2
4A
12
1
11

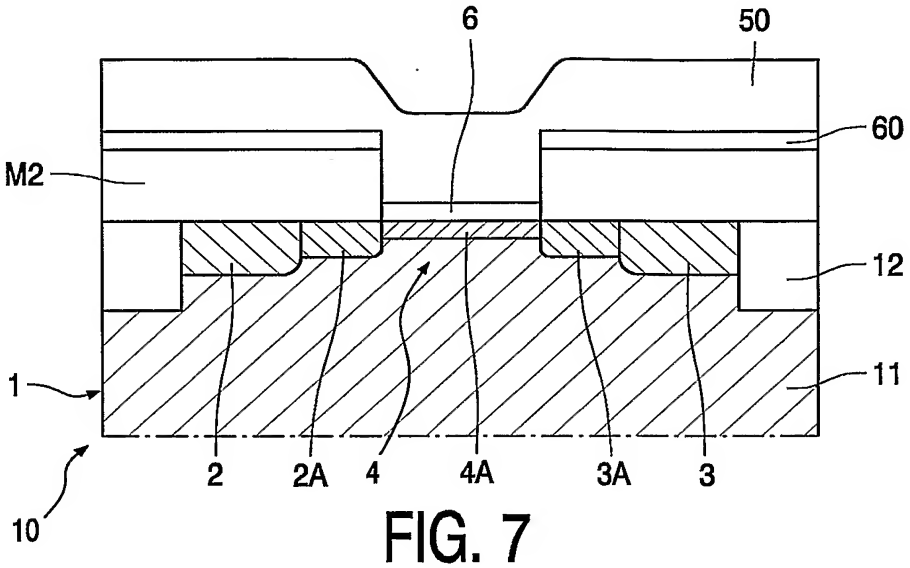


FIG. 7

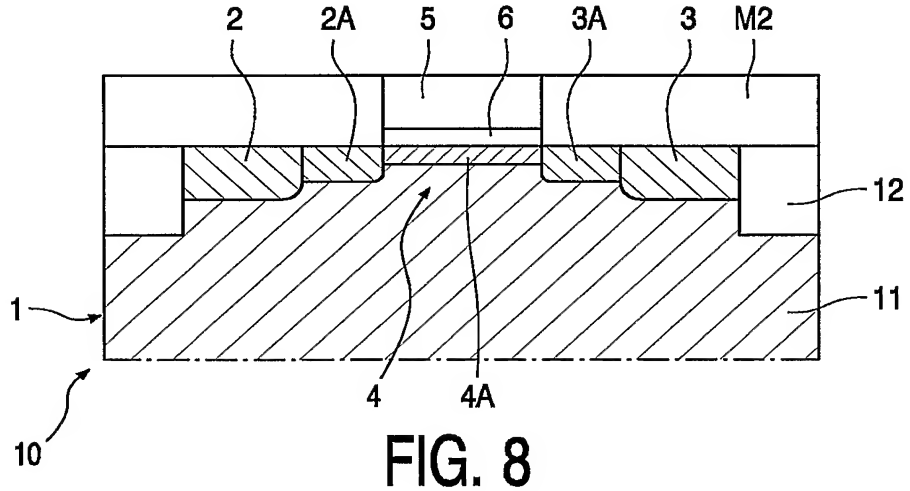


FIG. 8

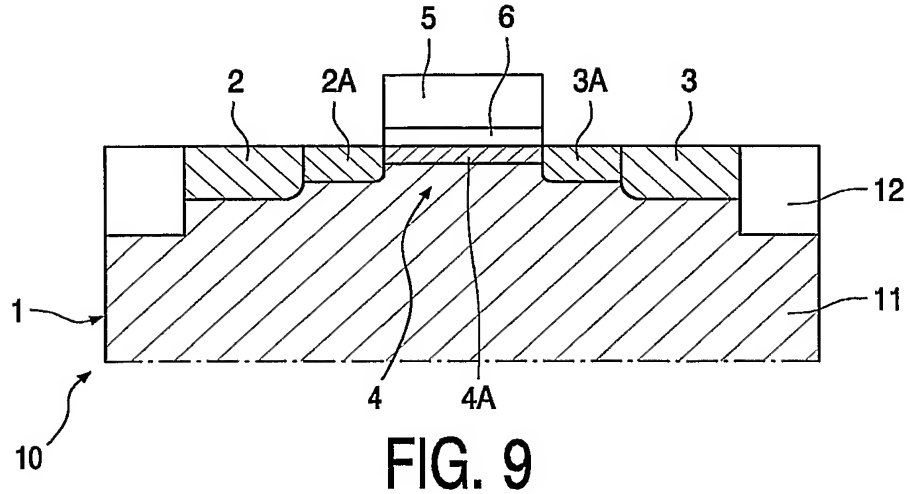


FIG. 9